

ISBN: 9788183715096

Digital Principles and System Design

P. Raja

Associate Professor

Department of Electronics and Communication Engineering

Sri Manakula Vinayagar Engineering College

Madagadipet

Pudhucherry - 605 107



Publishing for future

SCITECH PUBLICATIONS (INDIA) PVT. LTD.

www.scitechpublications.com

Contents

Chapter 1	Number System and Codes	1.1 - 1.77
1.1	Introduction	1.1
1.1.1	Analog system and digital system	1.2
1.1.2	Advantages of digital system	1.2
1.1.3	Limitation of digital systems	1.2
1.1.4	Comparison of analog and digital systems	1.3
1.2	Digital Principle	1.3
1.3	Number Systems	1.6
1.3.1	Decimal number system	1.6
1.3.2	Binary number system	1.7
1.3.3	Octal number system	1.8
1.3.4	Hexadecimal number system	1.8
1.4	Number System Conversions	1.8
1.4.1	Decimal to any BASE number system conversion	1.9
1.4.2	Any base number system to decimal number system	1.15
1.4.3	Binary to octal number	1.17
1.4.4	Octal to binary number	1.18
1.4.5	Binary to hexadecimal number	1.18
1.4.6	Hexadecimal to binary number	1.19
1.4.7	Octal to hexadecimal number	1.20
1.4.8	Hexadecimal to octal number	1.20
1.5	Binary Arithmetic	1.21
1.5.1	Binary addition	1.21
1.5.2	Binary subtraction	1.22
1.5.3	Binary multiplication	1.23

1.5.4	Binary division	1.23
1.6	Representing Signed Binary Numbers	1.24
1.7	Complements	1.26
1.7.1	Diminished radix complements or $(r - 1)$'s complements	1.27
1.7.2	Radix complements	1.28
1.8	Subtraction using complements	1.30
1.9	Comparison between 1's and 2's Complements	1.36
1.10	Sign Bit Overflow	1.36
1.11	Hexadecimal Arithmetic	1.37
1.11.1	Hex addition	1.38
1.11.2	Hex subtraction	1.39
1.12	Binary Coded Decimal (BCD)	1.40
1.12.1	8421 BCD code	1.40
1.12.2	BCD addition	1.41
1.12.3	BCD subtraction	1.42
1.13	Weighted Binary Codes	1.43
1.14	Reflective Codes	1.44
1.15	Sequential Codes	1.44
1.16	Non Weighted Codes	1.44
1.16.1	Excess 3 code	1.44
1.16.2	Gray code	1.46
1.17	Alphanumeric Code	1.47
1.17.1	ASCII code	1.48
1.17.2	EBCDIC code	1.49
1.18	Error Detection Codes	1.50
1.19	Error Correcting Code	1.52
	Short Questions and Answer	1.62
	Short Answer Questions	1.72
	Review Questions	1.73
	Exercises	1.74

Chapter 2	Boolean Algebra and Logic Gates	2.1 - 2.87
2.1	Introduction	2.1
2.2	Basic Definitions	2.2
2.2.1	Boolean postulates	2.2
2.2.2	Huntington postulates	2.4
2.2.3	Two - valued boolean algebra	2.5
2.3	Basic Theorems and Properties of Boolean Algebra	2.6
2.3.1	Duality theorem	2.6
2.3.2	Basic theorems	2.7
2.3.3	DeMorgan's theorems	2.8
2.4	Reducing Boolean Expressions	2.11
2.5	Standard Forms of Boolean Expression	2.12
2.5.1	Sum of products (SOP)	2.13
2.5.2	Products of sums (POS)	2.13
2.6	Canonical and Standard Forms	2.13
2.6.1	Minterm	2.13
2.6.2	Canonical form for sum of product expression	2.14
2.6.3	Converting product terms to standard SOP	2.14
2.6.4	Maxterm	2.16
2.6.5	Canonical product of sum expression	2.16
2.6.6	Converting a sum terms to standard POS	2.17
2.7	Converting SOP to POS	2.18
2.8	Canonical SOP Expression from Truth table	2.19
2.9	Canonical POS Expression from a Truth table	2.20
2.10	Deriving Truth table from SOP Expression	2.21
2.11	Deriving Truth table from POS Expression	2.22
2.12	Simplification of Boolean Expressions	2.22
2.12.1	Algebraic simplification	2.23
2.12.2	Karnaugh map simplification	2.24
2.13	Plotting a Karnaugh Map	2.26

2.13.1	Plotting K-map from truth table	2.26
2.13.2	Plotting of canonical SOP form on K-map	2.27
2.13.3	Plotting a canonical POS form on K-map	2.28
2.13.4	Grouping of cells for simplification	2.28
2.13.5	K-Map simplification for product of sum form	2.34
2.14	Don't Care Conditions	2.36
2.15	Quine - Mc Clusky (or) Tabulation Method	2.38
2.16	Logic Gates	2.41
2.16.1	AND gate	2.41
2.16.2	OR gate	2.43
2.16.3	NOT gate	2.44
2.17	Derived Logic Gates	2.44
2.17.1	NAND gate	2.45
2.17.2	NOR gate	2.46
2.17.3	EX OR gate or XOR gate	2.47
2.17.4	EX NOR gate or XNOR gate	2.48
2.18	Universal Gates	2.49
2.19	Implementation of Logic Function Using Gates	2.50
2.19.1	Logic diagram from logic function	2.50
2.19.2	Logic function from logic diagram	2.50
2.19.3	Truth table from logic diagram or logic function	2.51
2.19.4	Analysis of logic circuits	2.54
2.20	NAND and NOR Implementation	2.55
2.20.1	Two level NAND-NAND implementation	2.55
2.20.2	Multilevel NAND circuits	2.58
2.20.3	NOR implementation	2.60
2.20.4	Multilevel NOR implementation	2.61
2.21	Multi-Output Gate Implementation	2.62
	Short Questions and Answer	2.74
	Short Answer Questions	2.83

	<i>Review Questions</i>	2.85
	<i>Exercises</i>	2.85
Chapter 3	Combinational Logic Circuits	3.1 - 3.83
3.1	Introduction	3.1
3.2	Design Procedure	3.2
3.3	Adder	3.2
3.3.1	Half adder	3.2
3.3.2	Full adder	3.4
3.4	Subtractor	3.6
3.4.1	Half subtractor	3.6
3.4.2	Full subtractor	3.7
3.5	4 bit Binary Parallel Adder	3.9
3.6	Ripple Carry Adder	3.11
3.7	Carry Look Ahead Carry Adder	3.13
3.8	Serial Adder	3.16
3.9	4-bit Subtractor	3.17
3.9.1	Subtraction using 1's complement method	3.17
3.9.2	4-bit subtractor using 2's complement	3.18
3.9.3	4-bit parallel adder/subtractor	3.19
3.10	BCD Adder	3.21
3.11	Binary Multiplier	3.23
3.12	Magnitude Comparator	3.25
3.12.1	One bit magnitude comparator	3.25
3.12.2	2 - bit magnitude comparator	3.26
3.12.3	4-bit magnitude comparator	3.28
3.13	Decoder	3.30
3.13.1	2 to 4 binary decoder	3.31
3.13.2	3 to 8 decoder	3.32
3.13.3	Expanding decoder	3.33

3.13.4	Combinational logic implementation	3.34
3.13.5	BCD to seven segment decoder	3.36
3.14	Encoder	3.39
3.14.1	Octal to binary encoder	3.40
3.14.2	Decimal to BCD encoder	3.41
3.14.3	Priority encoder	3.42
3.15	Code Converter	3.45
3.15.1	Binary to BCD converter	3.45
3.15.2	BCD to excess -3 code converter	3.48
3.15.3	Excess-3 code to BCD code converter	3.49
3.15.4	Binary code to gray code converter	3.51
3.15.5	Gray code to binary code converter	3.52
3.16	Multiplexer	3.54
3.16.1	4 to 1 Multiplexer	3.55
3.16.2	Quad 2 - input data selector	3.58
3.16.3	8 to 1 multiplexer	3.58
3.16.4	Boolean function implementation	3.60
3.16.5	Application of multiplexer	3.61
3.17	Demultiplexer	3.62
3.17.1	1 to 4 demultiplexer	3.62
3.17.2	1 to 8 demultiplexer	3.63
3.18	Parity Generation and Checking	3.69
3.18.1	Parity generator	3.70
3.18.2	Parity checker	3.71
	Short Questions and Answer	3.72
	Short Answer Questions	3.77
	Review Questions	3.78
	Exercises	3.79

Chapter 4	Sequential Logic Circuits	4.1 - 4.88
4.1	Introduction	4.1
4.2	Types of Sequential Circuits	4.2
4.3	Comparison between Combinational Circuits and Sequential Circuits	4.2
4.4	Comparison between Synchronous and Asynchronous Sequential Circuit	4.3
4.5	Latches	4.4
4.6	RS Latch	4.4
4.6.1	RS latch using NOR gates	4.4
4.6.2	RS latch using NAND gates or $\bar{R}\bar{S}$ Latch	4.6
4.7	Flip-Flops	4.7
4.7.1	Clocked RS Flip-flop	4.7
4.7.2	D Flip-flop	4.8
4.7.3	JK Flip-flop	4.9
4.7.4	T Flip-flop	4.11
4.8	JK Master Slave Flip-flop	4.12
4.9	Triggering of Flip-flop	4.13
4.9.1	Level triggering in Flip-flop	4.13
4.9.2	Edge triggering Flip-flop	4.14
4.10	Edge Triggered D Flip-flop	4.15
4.11	Edge Triggered JK Flip-flop	4.15
4.12	Excitation Tables	4.16
4.12.1	RS Flip-flop	4.17
4.12.2	JK Flip-flop	4.18
4.12.3	D Flip-flop	4.19
4.12.4	T Flip-flop	4.20
4.13	Characteristic Table	4.20
4.14	Asynchronous Inputs of Flip-flop	4.21
4.15	Flip Flop Conversions	4.22

4.15.1	Realization of D Flip-flop using SR Flip-flop . . .	4.23
4.15.2	SR flip to T Flip-flop	4.25
4.16	Parameters of Flip-flop	4.27
4.16.1	Clock parameters	4.27
4.16.2	Flip-flop timing	4.28
4.17	Counters	4.29
4.17.1	Types of counters	4.29
4.18	Asynchronous Counter	4.29
4.18.1	MOD -4 or 2 - bit asynchronous counter	4.29
4.18.2	MOD-8 or 3-bit ripple counter	4.30
4.18.3	Counters with MOD numbers less than 2^n	4.32
4.18.4	Design of divide-by-N ripple counter	4.33
4.18.5	MOD - 6 ripple counter	4.33
4.18.6	MOD - 10 ripple counter or decade counter or BCD counter	4.34
4.18.7	Advantages and disadvantages of asynchronous counters	4.35
4.19	Synchronous Counters	4.36
4.19.1	2 - bit synchronous binary counter	4.36
4.19.2	3-bit synchronous binary counter	4.37
4.19.3	4-bit synchronous binary counter	4.38
4.19.4	Synchronous versus asynchronous counter	4.40
4.19.5	Design procedure of synchronous counter	4.40
4.19.6	Modulus N counter	4.40
4.19.7	Lock out	4.44
4.19.8	Up/Down synchronous counter	4.47
4.20	Programmable Counters	4.55
4.21	Shift Registers	4.57
4.21.1	Classification of shift registers	4.57
4.21.2	Serial in serial out (SISO) shift register	4.58
4.21.3	Serial in parallel out (SIPO) shift register	4.60

4.21.4	Parallel in serial out (PISO) shift register	4.61
4.21.5	Parallel in parallel out (PIPO) shift register	4.62
4.21.6	Bidirectional shift register	4.62
4.22	Universal Shift Register	4.63
4.23	Applications of Shift Registers	4.65
4.24	Shift Registers Counters	4.65
4.24.1	Ring counter	4.66
4.24.2	Johnson counter	4.67
	<i>Short Questions and Answer</i>	4.76
	<i>Short Answer Questions</i>	4.82
	<i>Review Questions</i>	4.84
	<i>Exercises</i>	4.86
Chapter 5	Synchronous Sequential Logic Circuits	5.1 - 5.65
5.1	Introduction	5.1
5.1.1	Mealy model sequential circuit	5.2
5.1.2	Moore model sequential circuit	5.2
5.2	Analysis and Synthesis of Synchronous Sequential Circuits	5.3
5.2.1	Analysis of example sequential logic circuit	5.4
5.3	State Reduction	5.14
5.4	State Assignment	5.17
5.5	Design Procedure	5.21
5.6	Synthesis of Clocked Sequential Logic Circuits	5.21
5.7	Sequence Generator	5.24
5.7.1	Sequence generator using counters	5.25
5.7.2	Sequence generator using shift registers	5.30
5.8	Sequence Detector	5.32
5.9	Sequential Programmable Devices	5.56
5.9.1	Sequential programmable logic devices	5.56
5.9.2	Complex programmable logic device	5.56

5.9.3	Field programmable gate arrays (FPGA)	5.57
	<i>Short Questions and Answer</i>	5.59
	<i>Short Answer Questions</i>	5.62
	<i>Review Questions</i>	5.62
	<i>Exercises</i>	5.62

Chapter 6 Asynchronous Sequential Logic Circuits 6.1 - 6.61

6.1	Introduction	6.1
6.1.1	Fundamental mode circuits	6.2
6.1.2	Pulse mode circuits	6.2
6.2	Analysis Procedure	6.2
6.2.1	Transition table	6.4
6.2.2	Flow table	6.5
6.3	Circuit with Latches	6.6
6.3.1	SR latch using NOR gates	6.6
6.3.2	SR latch using NAND gate	6.8
6.3.3	Analysis of asynchronous sequential circuits with latches	6.9
6.3.4	Implementation of asynchronous sequential circuit using SR latch	6.12
6.4	Design Procedure	6.14
6.4.1	Derivation of primitive flow table	6.14
6.4.2	State reduction techniques	6.16
6.4.3	Reduction of primitive flow table	6.20
6.4.4	State assignment	6.21
6.5	Pulse Mode Asynchronous Sequential Circuits	6.29
6.6	Analysis of Pulse Mode Asynchronous Sequential Circuits	6.29
6.7	Design of Pulse Mode Asynchronous Sequential Circuits	6.32
6.8	Hazards	6.36
6.8.1	Hazards in combinational logic circuits	6.36
6.8.2	Classification of hazards	6.37

6.9	Conditions for Static Hazard	6.38
6.10	Prevention of Hazards in Logic Gates	6.38
6.11	Essential Hazards	6.40
6.12	Hazards in Asynchronous Sequential Logic Circuits	6.41
6.13	Algorithmic State Machines	6.50
6.13.1	Components of ASM chart	6.50
6.13.2	ASM block	6.52
6.14	Introductory Examples of ASM Charts	6.53
	<i>Short Questions and Answer</i>	6.57
	<i>Short Answer Questions</i>	6.59
	<i>Review Questions</i>	6.60
	<i>Exercises</i>	6.60

Chapter 7 Memory and Programmable Logic Circuits 7.1 - 7.52

7.1	Introduction	7.1
7.2	Basic Terms of Memory	7.1
7.3	Basic Memory Operation	7.3
7.4	Memory Classification	7.4
7.5	Random Access Memory	7.6
7.5.1	Timing waveform	7.8
7.5.2	Memory decoding	7.9
7.5.3	Coincident decoding	7.10
7.5.4	Basic construction of a binary cell	7.11
7.6	Random Access Memory (RAM)	7.12
7.7	Read Only Memory	7.14
7.7.1	General structure of ROM	7.15
7.7.2	Programming the ROM	7.16
7.7.3	Combinational circuit implementation	7.17
7.8	Memory Expansion	7.19

7.8.1	Word length expansion	7.19
7.8.2	Word-capacity expansion	7.21
7.9	Programmable Logic Array (PLA)	7.22
7.10	Programmable Array Logic	7.28
	<i>Short Questions and Answer</i>	7.42
	<i>Short Answer Questions</i>	7.48
	<i>Review Questions</i>	7.49
	<i>Exercises</i>	7.50
Chapter 8	Introduction to Verilog HDL	8.1 - 8.34
8.1	Hardware Description Language (HDL)	8.1
8.1.1	Logic simulation	8.1
8.1.2	Logic synthesis	8.1
8.2	VHDL and Verilog HDL	8.2
8.3	Verilog HDL	8.2
8.3.1	Module representation	8.2
8.3.2	Writing simple verilog HDL code for logic circuits	8.2
8.3.3	Writing verilog HDL for logic circuit with delays .	8.4
8.3.4	Writing verilog HDL code for boolean expression .	8.4
8.3.5	Writing verilog HDL code for truth table	8.5
8.4	HDL for Combinational Circuits	8.9
8.4.1	Gate level modelling	8.9
8.4.2	Verilog-HDL code for combinational logic circuits	8.10
8.4.3	Data flow modelling	8.19
8.4.4	Behavioral modelling	8.22
8.5	HDL for Sequential Circuits	8.23
8.5.1	Behavioral modelling	8.23
8.5.2	Procedural assignments	8.25
8.6	Verilog code for latches and Flip-flops	8.25
8.6.1	D latches	8.25

8.6.2	D Flip-flop	8.26
8.6.3	JK Flip-flop	8.27
8.7	Verilog HDL Code for State Diagram	8.28
8.8	Verilog Code for Registers and Counters	8.30
8.8.1	SISO shift register	8.30
8.8.2	SIPO shift register	8.31
8.8.3	Universal shift register	8.32
8.8.4	Synchronous counter	8.32
	Short Answer Questions	8.33
	Review Questions	8.34
	Index	I.1-I.4

SCITECH